10/607064

METHOD OF FORMING A TRENCH ISOLATION

BACKGROUND OF THE INVENTION

This application is a division of co-pending Application No. 09/986,142, filed on September 20, 2001, the entire contents of which are hereby incorporated by reference.

1. Field of the Invention

The present invention relates to a method of forming a semiconductor integrated circuit, and more particularly to a trench isolation in a semiconductor integrated circuit.

2. Description of the Related Art

Isolations for electrically isolating semiconductor devices are important for the semiconductor integrated circuit with a high withstand voltage. It was known that one or more trench isolations are formed in a silicon-on-insulator substrate. In the semiconductor integrated circuit with the high withstand voltage, a depth of the semiconductor devices may reach a few micrometers, for which reason it is necessary that the trench depth is ranged from a few micrometers to 10 micrometers.

Japanese laid-open patent publication No. 8-23027 discloses that TEOS(Tetra Etyl Ortho Silicate)-SiO_2 is filled within a trench groove in the silicon-on-insulator substrate. FIGS. 1A through 1D are fragmentary cross sectional elevation views illustrative of trench isolations in silicon-on-